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EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 02/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/977,140	BLEMEL, KENNETH G.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears n the cover sheet with the corresp ndence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-18 are presented for examination.

2. Claim 6 is objected to because of the following informalities: the monitoring device (line 4). It is believed that the monitoring device was meant to be the monitoring devices in line 2 of the preamble. Appropriate correction is required.

3. Claim 1 recites the limitation "the architecture" in line 16. There is insufficient antecedent basis for this limitation in the claim. Suggestion : is it referring to the FPGA architectures in line 12, or the one of the processing elements in lines 4-10 ?

4. Claim 8 recites the limitation "the system support applications" in line 1. There is insufficient antecedent basis for this limitation in the claim. Suggestion : a plurality of system support applications, or the like.

5. Claim 14 recites the limitation "said FPIC" in line 2. There is insufficient antecedent basis for this limitation in the claim.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jennings, III (6,449,273) in view of Wynn et al. (6,275,499).

7. As to claims 1,3, Jennings, III disclosed a field programmable instrument controller comprising at least :

a) a plurality of processing elements (see fig.4 [410a-d], see also channel processor 426 in 410) adapted to perform special tasks, each processing element was a function represented by software programs or algorithms (not explicitly shown, but see the programmable logic device, see also program code stored in the memory in col.4, lines 25-41) , or by specific hardware, or firmware controlled (microprocessor), or by state machine (finite state machine), or combinatorial asynchronous or sequential Boolean logic , or programmable array (FPGA) each processing element being activated on fly to communicate with other (see col.4, lines 14-27, see the communication in col.5, lines 13-31, see also the programmability of the processor in col.5, lines 1-12, se also the interconnection among the processors in col.7, lines 1-11) ;

wherein the processing elements operate in parallel and serial (see parallel and serial) in plurality of architecture s instantiated on fly by field programmable gate array (see the FPGA in col.4, lines 20-25, see also the serial bus USB for background in col.1, lines 11-21, see also the multiple communications channels processed concurrently in col.2, lines 66-67, col.6, lines 5-12, lines 18-26);

the computing architecture being bi size (see the background of bit stream in physical layer in col.1, lines 55-64, see also the bit communications in col.4, lines 46-55) and functional defined in a program definition algorithm (see the control program) stored in a memory for the purpose of embodiment of that architecture in a portion of the FPGA

(see the memory for storing the program to initialize the processor and the program codes in col.4, lines 20-41);

At least one processing unit is capable of interact with other controller (see the external interface in col4, lines 57-65);

The processing element which all or several assumed the roles to create required process control function, whereby at least one processing element represent the specific function of the memory allocation and retrieval(see the cache controller 428 in col.4, lines 26-41) , at least one processing element interconnected with real time processing and hardware (sees port circuit [436] the analog to digital conversion in col.4, lines 50-56, see also the DSP, the real time in col.4, lines 14-18), at least one processing element covered specific function related to control process (see the cache controller 428 in any of the processor 410), at least one processing element function as access point to external extension (see channel interface 440 with I/O buffer and the external interface 442 in col.4, lines 57-65).) selected form group of microprocessors, flash , microprocessor, network, data busses (see the FLASH, microprocessor, micrococntroller in col.4, lines 20-41, see the modular design in col.6, lines 28-50 for the macro processor , see also the interrupt controller to trigger the network conditions in col.4, line s14-19, see also col.5, lines 13-31 for interprocessor communications, see also col.6, lines 27-50 for network connections and data buses).

8. Jennings , III did not specifically show the PCMIA as claimed. However, Wynn disclosed a PCMIA (see fig.19 [PCMIA], col.15, lines 38-47). It would have been obvious to one of ordinary skill in the art to use Wynn in Jennings , III for including

PCMIA as claimed because the use of Wynn could provide Jennings , III the interface capability to adapt to additional system expansion, such as the PCMIA bus, and therefore, increasing the system structure of the processing element in Jennings, and it could be achieved by predefining the R/W ports of the PCMIA of Wynn into the configuration file of Jennings, III so that the connection of PCMIA of Wynn could be recognized by Jennings, III in order to achieve the enhanced system structure, and for the above reason, provided a motivation. Jennings , III is used as primary reference because it showed clearly a plurality of processing elements in a field programmable circuit.

9. As to the claim language "on the fly", it is read as real time processing, and Jennings , III did disclose real time processing (see the analog to digital conversion and the DSP).

10.

11. As to claim 2, Jennings , III also included a common access point (see fig.3 [300]).

12. AS top claim 4, see the micro controller, programmable logic devices, finite state machine in col.4, lines 20-41, see also col.5, lines 1-12).

13. As to claim 5, col.2, lines 12 (asynchronous, ATM), col.4, lines 14-19 (interrupt and clock timer for synchronous), see also the communication control and status thought the separate communication mechanisms for col.1, lines 11-26, col.6, lines 5-26 for the serial bus and concurrent data transfer the asynchrous and synchronous in serial and parallel fashion.

14. As to claim 6, claim 6 is dependent from claim 1 because it has the dependent feature from claim 1 (see claim 6, lines 16-17). Applicant's feedback regarding the dependency of the claim 6 is welcome in the next response. Jennings also included at least sensors (see analog to digital conversion in col.4, lines 42-50), a local data processor for receiving data from the sensors (see processor [436] coupled to communication channels in col.4, lines 46-55), and a centralized processor [320] [400] coupled to plurality of local devices [see communication channels 13] for weighing parameters and diagnosing (weighing parameters and diagnosing not explicitly shown, but see the laser signals conversions in col.4, lines 49-56, see also but see fig.3 320, see also processor 400 can operate as processor 320 in col.3, lines 41-68, see the detailed control operations in col.5, lines1-31).

15. As to claim 7, Jennings s , III also included at least :

a) first control for specific functionality of system support (see the support circuit 436);

2) second process control covered all applications related to real time networks (se the real time actions in col.4, lines 14-19),

3) third process included human interface applications (see the I/O analog conversion incol.4, lines 46-55);

4) LAN and WAN (see LAN and WAN for the background in col.1, lines 11-26).

16. As to the wireless, Wynn also taught wireless (see col.4, lines 40-47).

17. As to claim 8, Wynn also included at least a fault handling (see col.31, lines 34-47). No specific format of the power management , wake-up, vitality control has been reflected into the claim, therefore, it is assumed they are general type of power

management, such as power on and off (both teachings in Jennings, III and Wynn), general save mode (not explicitly shown), and the analog signals for the A/D conversions (see Jennings , III, col.4, lines 46-55).

18. As to claim 9, Jennings also included electro-optic (see the laser in col.4, lines 46-57). As to the electro mechanic and electro-hydraulic, no specific format or the type of the electromechanically and hydraulic systems has been reflected into the claim, therefore, it is assumed any system element which was capable of using the relevant functionalities, such as Jennings, III taught a laser converter (see col..4, lines 46-57), laser converter must connected from a laser gun , or the like, therefore, it must have involved with some mechanical and hydraulic mechanisms, although Jennings, III did not explicitly show the mechanical and hydraulic systems, one of ordinary skill in the art should be able to recognize the need of using a mechanical and hydraulic mechanism in general sense to support the laser beans or the laser signals.

19. As to claim 10, Jennings, III taught the analog to digital converter and DSP which encompassed the physical and visual and voice inputs and outputs.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 11-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Staiger (6,292,718).

20. AS to claim 1, Staiger disclosed a system (see fig.8) comprise g at least :

a) one control apparatus [c1] in communication with a plurality of other electronic processors [c2]-[c4] each performed a specific task (see col.7, lines 1-31 for the brief descriptions performed by each of the control elements c1-c4) each of which was able to communicate the remaining control elements (see Abstract, col.12, lines 66-67, col.13, lines 1-3, see also fig.8, col.15, lines 13-37 for details).

21. As to claim 12, Staiger also included standard data link or physical representation (see col.11, lines 10-31);

22. As to claim 13, Staiger also included arbitrated link with standard bus technique (see col.11, lines 32-47).

23. As to claim 14, Staiger also implemented in software of the processors (see the software implementation in col.7, lines 34-42, lines 44-50, see also the software implementations in c1, c2, c3,and c4 in col.7, lines 34-67, col.8, lines 1-62, col.9, lines 4-55).

24. As to claim 15, Staiger also included the combination capability of the other control elements (see col.9, lines 59-67, col.10, lines 1-67 for the cooperative operations of the control elements , see also col.11, lines 61-67, col.12, lines 1-16, fig.8 for the combination ability of the control elements).

25. As to claim 16, Staiger also included a tetrahedral interconnection (see fig.8, see col.15, lines 20-25).

26. As to claim 17, Staiger also included a real time ECU (see the real time in col.6, lines 31-39).

27. As to claim 18, Staiger also included secure access via a network and wireless (see the secure solution in col.6, lines 32-39).

28. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Bell et al. (5,892,767) is cited for the specifc teaching of the combination of a plurality of the programmable logic processing elements with external connections (see col.6, lines 66-67, col.7, lines 1-10).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

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21 Century Strategic Plan

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